Microchip

ER59256

256 Bit Serial Electrically Erasable/Programmable ROM

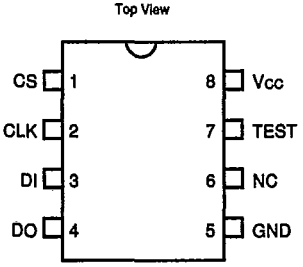
FEATURES

- Low cost
- 16 x 16 serial EEPROM
- Single +5V only operation
- Binary addressing
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word.
- Power on/off data protection circuitry
- Available for extended temperature ranges:
  — Commercial: 0°C to +70°C
  — Industrial: -40°C to +85°C

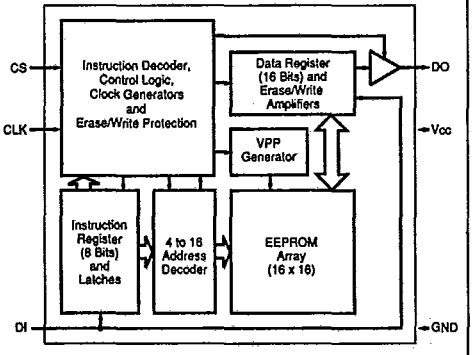
DESCRIPTION

The ER59256 is a low cost, serial EEPROM manufactured in Microchip's highly reliable SNOS technology. The key features of this device are its +5V only operation and microcomputer compatible architecture. Six 9-bit instructions can be executed. See Table 1. The instruction format has a logical "1" as a start bit, four bits as an opcode, and four bits of address.

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to ground ..... -0.3V to +7.0V
Storage temperature (unpowered and without data retention) ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... 1.0KV (typical)

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
Vcc	+5V Power Supply
GND	Ground
NC	No Connect
TEST	Must tie to Ground

DC CHARACTERISTICS

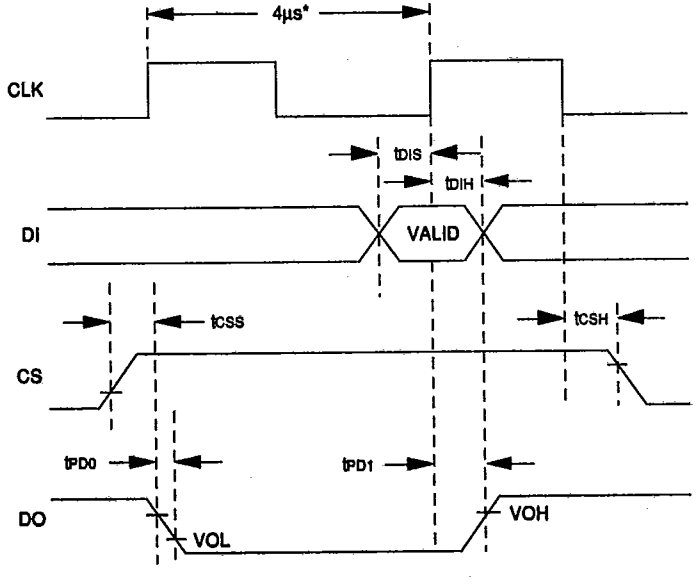
Vcc =+5V± 10%
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C

Parameter	Symbol	Min	Max	Units	Conditions
Input Voltage					
High Level	V_{IH}	2.0	Vcc+1.0	V	
Low Level	V_{IL}	-0.3	+0.8	V	
Output Voltage					
High Level	V_{OH}	2.4	Vcc	V	I_{OH} = -400µA
Low Level	V_{OL}	—	0.4	V	I_{OL} = 1.6mA
Leakage Current					
Input	I_{LI}	—	+10	µA	V_{IN} = GND to Vcc
Output	I_{LO}	—	+10	µA	V_{OUT} = GND to Vcc
Current					
Operating	I_{CC1}	—	10	mA	Vcc = 5.5V, CS = 1
Standby	I_{CC2}	—	3	mA	Vcc = 5.5V, CS = 0
Erase/Write Operating	I_{CC3}	—	12	mA	Vcc = 5.5V
Power Consumption					
Operating	P_{CC1}	—	55	mW	Vcc = 5.5V, CS = 1
Standby	P_{CC2}	—	17	mW	Vcc = 5.5V, CS = 0
Erase/Write	P_{CC3}	—	66	mW	Vcc = 5.5V, CS = 1

AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock Frequency	fCLK	0	250	kHZ	
Clock Duty Cycle	DCLK	25	75	%	
Chip Select Setup Time	tCSS	0.2	—	µS	
Chip Select Hold Time	tCSH	0	—	µS	
Data Input Setup Time	tDIS	0.4	—	µS	
Data Input Hold Time	tDIH	0.4	—	µS	
DO Output Delay (H to L)	tPD0	—	2.0	µS	CL = 100pf
DO Output Delay (L to H)	tPD1	—	2.0	µS	CL = 100pf
Erase/Write Pulse Width	tE/W	10	30	ms	
Input Capacitance	CI	—	6	pf	VIN = 0V
Output Capacitance	CO	—	10	pf	VOUT = 0V

FIGURE 1 SYNCHRONOUS DATA TIMING



* This is the maximum clock frequency.

FUNCTIONAL DESCRIPTION

TABLE 1 INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	1	1000	A3A2A1A0	D15-D0	Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0	—	Erase Register A3A2A1A0
EWEN	1	0011	0000	—	Erase/write enable
EWDS	1	0000	0000	—	Erase/write disable
ERAL	1	0010	0000	—	Erase all registers

DI/DO Pins

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

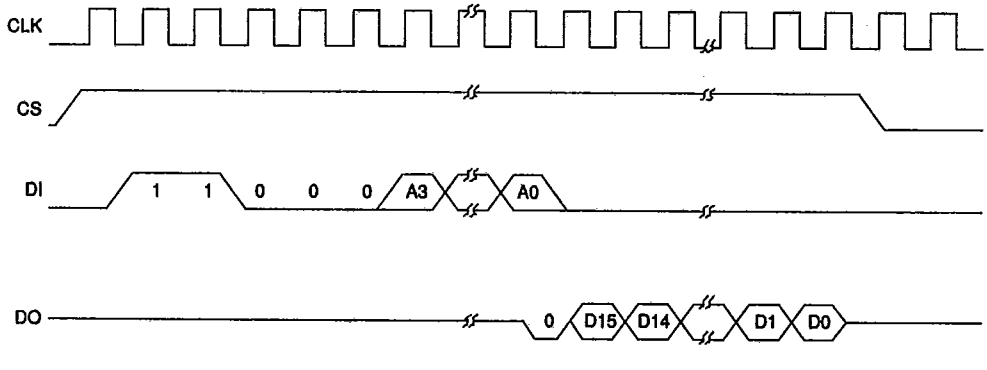
Power On/Off Data Protection Circuitry

During power-up modes of operation are inhibited until Vcc has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the voltage range of 2.8 to 3.5 volts.

Read

The READ instruction is the only instruction which outputs serial data on the DO pin. Only during the READ mode is the output pin (DO) valid. During all other modes the DO pin is in tri-state, eliminating bus contention. A dummy bit (logical "0") precedes the 16-bit output string. The output data changes during the high state of the system clock.

FIGURE 2 READ MODE



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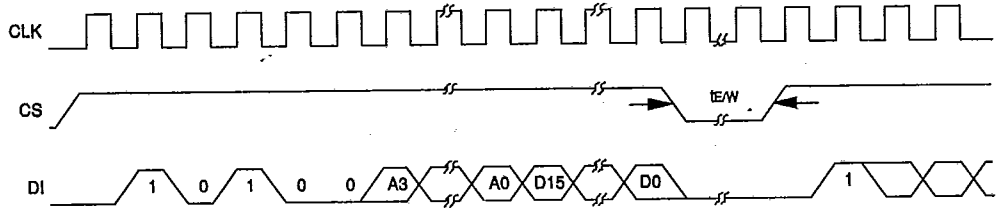
Write

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one CLK period, or followed by another instruction.

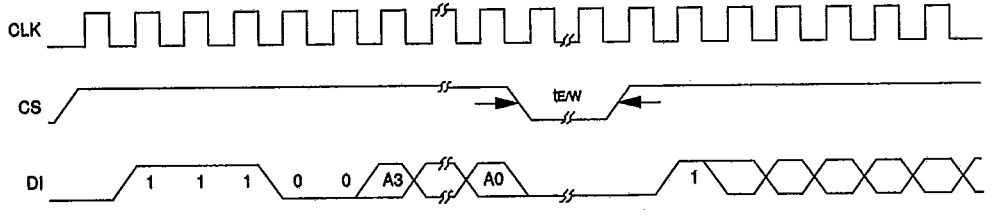
FIGURE 3 WRITE MODE



Erase

Like most EEPROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($T_{E/W}$) constraint has been satisfied, CS is brought up for at least one CLK period. a new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

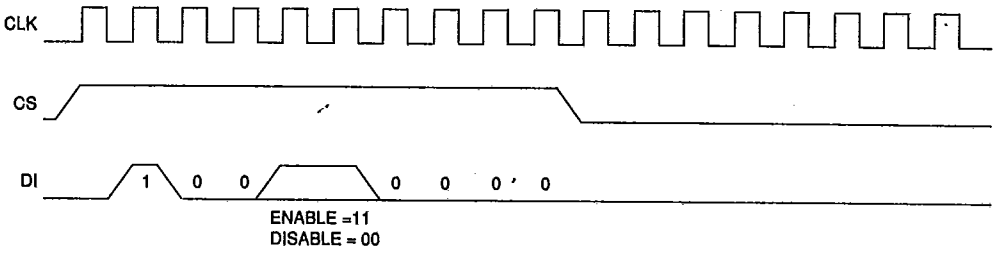
FIGURE 4 ERASE MODE



Erase/Write Enable

Programming must be preceded once by an Erase/Write Enable (EWEN) instruction. Programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions. The device powers up in the Erase/Write Disable (EWDS) Mode.

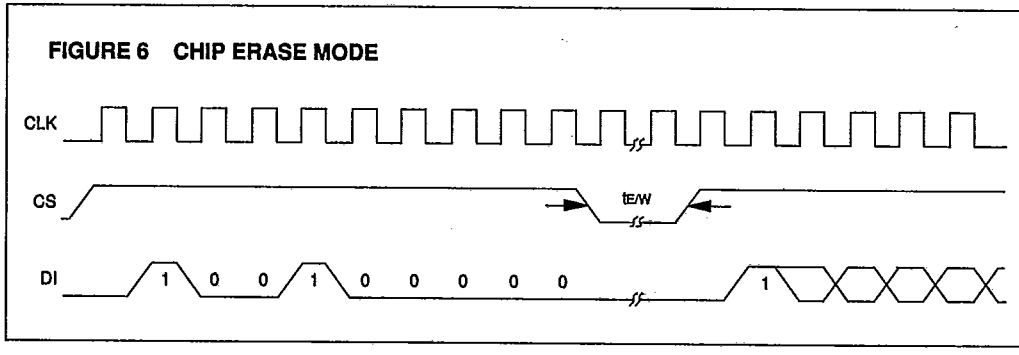
FIGURE 5 ERASE/WRITE ENABLE AND DISABLE



Chip Erase

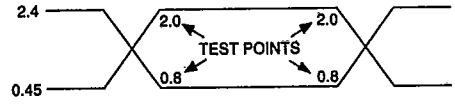
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

FIGURE 6 CHIP ERASE MODE



TESTING WAVEFORMS

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0"

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

ER59256 -I /P

Package:	J	CERDIP
	P	Plastic DIP (OTP Available)
Temperature Range:	Blank	0°C to 70°C
	I	-40°C to 85°C
Device	59256	256 Bits SNOS Serial EEPROM