GENERAL INSTRUMENT

ER1400

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

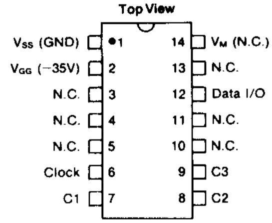
- 100 word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Single −35 Volt supply
- Word alterable
- 10 year data storage
- MOS compatible signal levels
- Write/erase time: 10ms

PIN CONFIGURATIONS

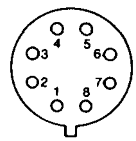
Standard package
14 LEAD DUAL IN LINE

Special Order Package
8 LEAD TO-8 (ER1400T)

Top View



Bottom View



1. Data I/O
2. V_M (N.C.)
3. V_{SS} (GND)
4. V_{GG} (−35V)
5. Clock
6. C1
7. C2
8. C3

N.C.= No external connection for normal usage

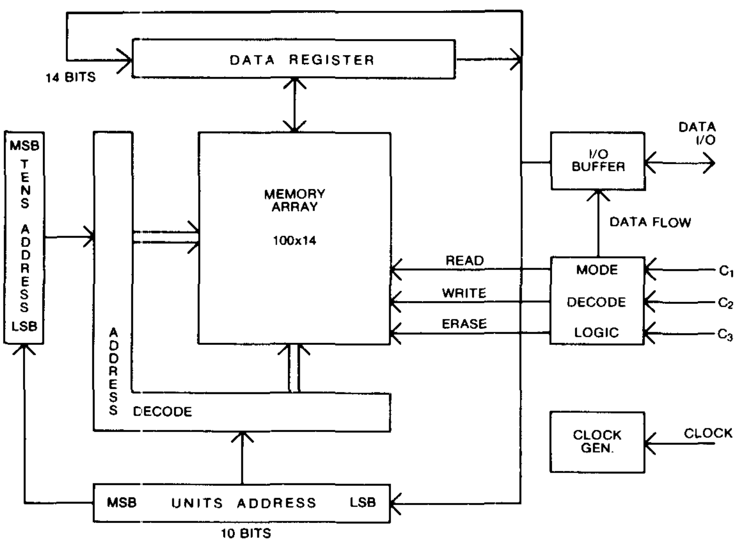
DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. When outputting data it has MOS drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to V_{SS} −35 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby—the output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.
0	1	1	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read—The address word is read from memory into the data register.
1	0	1	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase—The word stored at the addressed location is erased to all ones.
1	1	1	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write—The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V_{GG}) with respect to V_{SS} . . −20V to +0.3V
V_{GG} with respect to V_{SS} . . . . −40V
Storage temperature (No Data Retention) . . . . −65°C to +150°C
Storage temperature (with Data Retention)
Operating . . . . −25°C to +75°C
Unpowered . . . . −65°C to +80°C

Standard Conditions (unless otherwise noted):
V_{SS} = GND
V_{GG} = −35V ±8%
Operating Temperature T_A = 0°C to +70°C

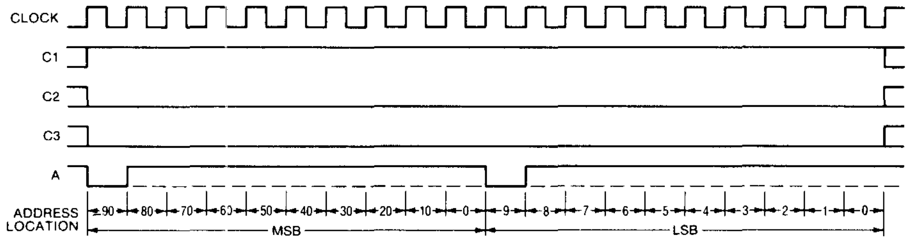
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	V_{IL}	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	V_{IH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	V_{OL}	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	V_{OH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	$f\phi$	10.0	14.0	17.0	kHz	
Clock duty cycle	$D\phi$	35	50	65	%	
Write time	tw	10.0	15.0	24.0	ms	
Erase time	te	10.0	15.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	μs	
Propagation delay	tpw	—	—	20.0	μs	Load – 1 Meg, 100pF
Non-volatile data storage	T_S	10	—	—	Years	See Note 1.
Number of erase/write cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.
NOTE 1: T_S is for powered or unpowered storage.
NOTE 2: N_W (=10^4) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprogramming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

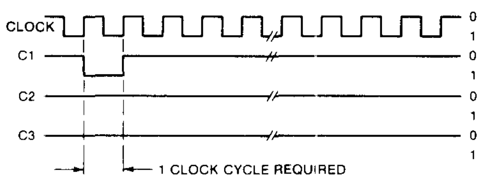
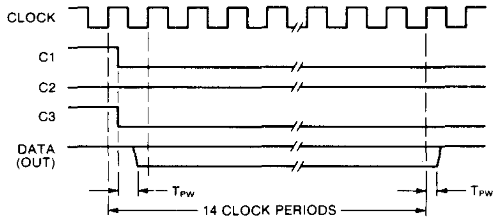


Fig.2 READ



T_{PW} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at $V_{SS}-2$ and -10 volt points.

Fig.3 SHIFT DATA OUT

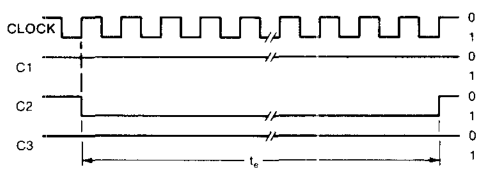


Fig.4 ERASE

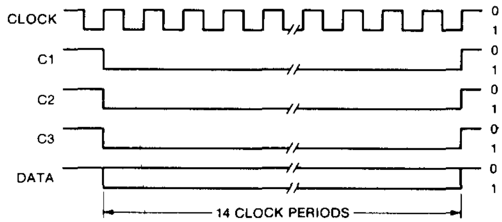


Fig.5 ACCEPT DATA

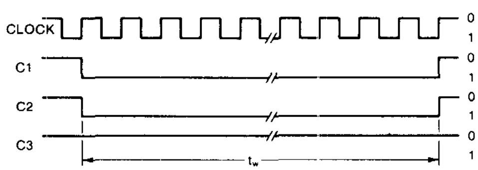


Fig.6 WRITE

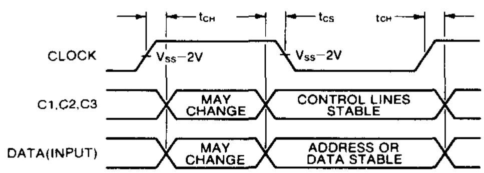


Fig.7 INPUT TIMING

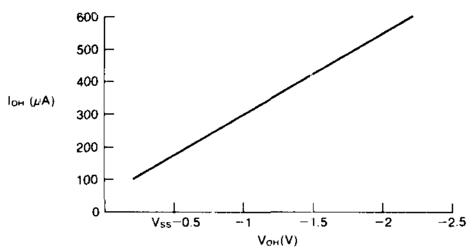


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

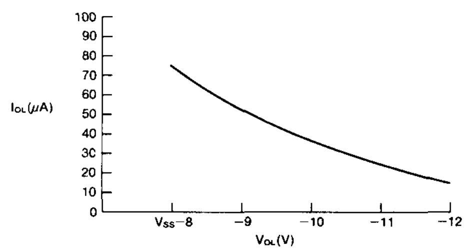


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Economega IV TV PPL Tuning System Control

FEATURES

- 100 Channel Tuning Capability — Includes CCIR Standard Channels, Italian and German Cable Channels
- 32 Favorite Program Storage in Non-Volatile Memory (ER1400)
- Automatic Sweep Tuning Option (with Automatic Fine Tune)
- *Fine Tune in 50KHz Steps (Manual or Automatic)*
- Two Digit Channel Number Display
- Two Digit Program Number Display
- Fast Lock Up Time, 10ms (typ)
- Parallel Remote Control Input
- 38.9MHz IF
- Easily Reprogramed for Different Channels (e.g. U.S.A.), Features and Interfaces. (Inquire for Alternative Versions)

DESCRIPTION

This specification describes a PIC1650-020 microcomputer which is used as a control chip in a phase locked loop television tuning system. The microcomputer interfaces with a number of sub-systems which are detailed below.

1. AY-3-8475 I.R. Receiver. The PIC1650-020 accepts program numbers from the receiver thus allowing remote program selection.
2. ER1400. Electrically Alterable ROM. The ER1400 is used to store Channel, Fine Tune and AFT data for each program. Information is stored and recalled by the PIC1650-020 as required.
3. CT2012 Frequency Synthesizer. The PIC1650-020 sends frequency and band data to the synthesizer. This data is ultimately used to determine the local oscillator frequency. The PIC1650-*020 also controls the AVIN signal to the synthesizer chip.*
4. CT2017 Tuning Interface. Signals from this chip are monitored by the PIC1650-020 when operating in CHANNEL SWEEP or AUTO MODES. The Tuning Interface chip also controls the PIC1650-020 master clear input via an external inverter.
5. User controls including SN7447A, BCD to Binary decoder/driver.
   (a) Four 7 segment displays which are used to display Program and Channel information.
   (b) One LED to indicate if AUTO mode is selected.
   (c) Seven push button switches for channel selection, local Program Selection, Fine Tuning and AUTO Mode selection.
6. The PIC1650-020 supplies a MUTE signal to mute the TV sound during Program and Channel change.

OPERATION

Program Selection (A0-A5)

32 remote programs can be entered via inputs (A0-A4) from the I.R. receiver AY-3-8475. These lines contain valid program information only when the STROBE input (A5) is low. Information on A0-A4 is in the range 0-31 representing programs 1-32 respectively.

The PIC1650-020 will tune the TV to a new program only if the STROBE is low and the program data on A0-A4 is different from the current program data.

Program numbers are used to address the ER1400 allowing the user to allocate a TV channel to each program.

The TV sound is muted for 600ms at each program change.

Changes in program number are ignored if any of the local switches are pressed.

ER1400 Interface (B0-B4)

To enable the ER1400 inputs to be pulled high to V_{XX}, PIC1650-020 pins (B0-B4) have open drain outputs with external pull up resistors as shown in Fig. 2.

The ER1400 contains 100 words of 14 bits. Two words are needed to store the 17 bits of information required for each program.

CHANNEL information for PROGRAM N is stored at ER1400 address N. The corresponding FINE TUNE NUMBER and AFT information is stored at address N +40.

Address Formats

Address	MSB	DATA	
N	XX XXXX	CT.CT.CT.CT.	CU.CU.CU.CU.
N + 40	XX XXXAFT	FT.FT.FT.FT.	FT.FT.FT.FT.

X = Not Used
CT = BCD digit for CHANNEL TENS data
CU = BCD digit for CHANNEL UNITS data
AFT = AUTO/MANUAL mode. AFT = 1 = AUTO mode
FT = FINE TUNE NUMBER

Data is written to the ER1400 when:

1. Either the CHANNEL TENS or CHANNEL UNITS switch is released.
2. Either the FINE TUNE UP or FINE TUNE DOWN switch is released.
3. AUTO switch is pressed.
4. AUTO mode is entered from CHANNEL SWEEP.

Data is read from the ER1400 when a new program is selected. The data is converted to a suitable format and then transferred to the synthesizer. If the Channel data read from the ER1400 is not a valid BCD number then the channel number is set to 00. Under these conditions it is likely that the Fine Tune data from the ER1400 will also be non-valid. No attempt is made to correct this data. It is sent to the synthesizer as read from the ER1400.

Frequency Synthesizer Interface (B6, B7, C0-C3)

AVOUT — (B6)

This output is normally low and goes high when programs 16 or 32 are selected. It is routed via the synthesizer and can be used to modify the time constant of the video synchronizing circuit of the television for use with video recorders.

Data Highway & Clock — (B7, C0-C3)

Tune information is transferred to the synthesizer on a 4 bit highway which is shared with the display decoder/driver. The synthesizer ignores data on the highway unless a clock is present. Clock signals (SYN CLK) are generated by the PIC1650-020 as required. A timing diagram is shown in Fig. 3.

When the power is initially switched on 16 clock pulses, with random data, are sent to initialize the synthesizer. Under normal operating conditions 11 clock pulses are required to transfer Tune data and 5 clock pulses are required to transfer Fine Tune Data.

TUNE DATA FORMAT

	H3	H2	H1	H0	
SC1	0	0	0	1	Control Code to synthesizer
SC2	1	1	0	1	
SD1	0	0	0	0	
SD2	0	0	0	0	
SD3	0	0	0	0	
SD4	B1	B0	Q9	Q8	Band and Frequency Number Data
SD5	Q7	Q6	Q5	Q4	
SD6	Q3	Q2	Q1	Q0	
SD7	0	0	0	R4	Fine Offset data
SD8	R3	R2	R1	R0	
SC3	X	X	X	X	Not Specified

NOTES:

1. Band Information is coded as follows:

B1	B0	
0	0	BAND 1 — VHF I
0	1	BAND 3 — VHF III
1	0	BAND 4 — UHF
1	1	BAND 2 — NOT USED

2. Q9-Q0 is a *binary number* representing the required tune frequency in MHz. The frequency is in the range 84MHz to 914MHz. Q9 is the most significant bit.
3. R4-R0 is a binary number in the range 0-19. This is used to modify the tune frequency in 20 steps of 50KHz. R4 is the most significant bit. An increase in the Fine Offset number means a corresponding decrease in frequency.

FINE TUNE DATA FORMAT

	H3	H2	H1	H0	
SC1	0	0	0	1	Control Code to Synthesizer
SC2	1	1	1	0	
SD1	F7	F6	F5	F4	FINE TUNE NUMBER Data
SD2	F3	F2	F1	F0	
SC3	X	X	X	X	Not Specified

NOTES:

1. F7-F0 is a binary coded modular 20 number which is used to modify the tune frequency in 160 steps of 50KHz. F7 is the most significant bit. An increase in the Fine Tune Number means a corresponding decrease in frequency.

Tuning Interface (CT2017)

UP and DOWN (A6, A7)

These inputs are derived from an AFC circuit within the television. They perform two functions. They signal a Stop Sweep when in CHANNEL SWEEP and they control the television Fine Tuning when in AUTO mode.

Master CLear (MCLR)

The PIC1650-020 Master Clear signal is controlled via an external inverter by the POWER ON DET signal from the Tuning Interface chip. The Master Clear signal must be held low for at least 1ms after all power supplies become valid. When the Master Clear signal goes high the PIC1650-020 will tune the TV to the channel allocated to Program 1.

User Controls

Four common anode 7 segment displays are used to display Channel and Program information. Two digits are used to display channel information in the range 00 to 99. Leading zeros are not blanked. The remaining 2 digits display the selected program. Program information lies in the range 1-32. Leading zeros are blanked.

Digits are displayed in turn by enabling 1 of the 4 digit driver transistors (C4-C7) and simultaneously outputting the corresponding segment code on C0-C3. Each digit is enabled for approximately 3ms in any 12ms period.

As the segment outputs share a common highway with the synthesizer the display is blanked, by switching off all 4 digit drivers, during a data transfer to the synthesizer. This blanking is not noticeable during normal operation.

It is not possible to maintain the displays when writing to the ER1400. Displays are blanked for 80ms each time a WRITE takes place.

Seven push button switches are mounted on the front panel. Only one switch is serviced at any one time, all other switches being inhibited until the current switch is released.

The following functions are controlled by the switches:

1. Increment Channel Tens
2. Increment Channel Units
3. Fine Tune Up
4. Fine Tune Down
5. Program Step
6. Channel Sweep
7. Auto

Increment Channel TENS or UNITS (D0, D1)

These switches enable the television to be tuned to any of 100 channels in the range 00-99.

Closure of the Channel Tens switch causes the Channel Tens display to increment one step and thereafter one step every 0.5 sec, overflowing from 9 to 0, until the switch is released. At each step the appropriate TUNE data is transferred to the synthesizer and MUTE is activated for 600ms.

Closure of the Channel Units switch causes the Channel Units to increment similarly, there being no overflow to Channel Tens.

In both cases, at every step, the Fine Tune Number is set to its mid-point (128) and transferred to the synthesizer.

On release of either switch the current channel and Fine Tune Number are stored at the appropriate ER1400 address.

Fine Tune Up and Fine Tune Down (D3, D4)

Closure of a switch causes a single Fine Tune step, in the appropriate direction, to be executed. This is followed by a pause of 0.4 sec, thereafter steps occur at 50ms intervals. The pause allows single step Fine Tuning to be carried out. At each step the new Fine Tune Number is transferred to the synthesizer.

On release of the switch current Channel and Fine Tune Number are stored at the appropriate ER1400 address.

NOTE: Fine Tune Up means decrease in Fine Tune Number which gives a corresponding increase in frequency.
Fine Tune Down acts in a similar fashion.

The Fine Tune Number allows tuning of +4MHz, −3.95MHz, in 50KHz steps around the allocated channel frequency.

Program Step (D6)

Closure of the Program Step switch causes the displayed program number to increment one step and thereafter one step every 0.5 sec, overflowing from 32 to 1, until the switch is released. At each step the channel display is updated and the appropriate TUNE information is sent to the synthesizer. The MUTE signal is activated for 600ms at each step.

Channel Sweep (D5)

The Channel Sweep enables the user to sweep through each channel in turn (in order of increasing Channel Number, with roll over from 99 to 00) stopping when a valid stop signal, as indicated by the UP and DOWN inputs, is detected. The sweep is implemented by decrementing the Fine Tune Number in steps of 5, at 12ms intervals, which is equivalent to increasing the frequency in steps of 250KHz.

Band 1 and Band 3 channel widths are 7MHz and are swept −3.45MHz, +3.3MHz around the allocated channel frequency. UHF band channel widths are 8MHz and are swept −3.95MHz, +3.8MHz around the allocated channel frequency.

When the switch is initially closed the sweep starts from the bottom of the next channel. A pause of 250ms is initiated before continuing. On succeeding channel boundaries there is a 12ms pause unless a bank change is involved in which case there is a 0.5 sec pause.

For normal operation the sweep switch should be closed momentarily and then released. If the switch is held closed and a STOP is detected, AUTO mode is entered where the appropriate Channel and Fine Tune data is stored in the ER1400. At this point because the sweep is closed, the sweep is restarted from the bottom of the next channel.

The sweep mode can be terminated at any time by pressing any of the push buttons (other than CHANNEL SWEEP) on the front panel or by selecting a new program. A STOP signal, indicating a TV station has been found, is recognized by UP going high then low followed by DOWN going high (Fig. 4). When a TV station is found the PIC1650-020 enters the AUTO mode.

Auto (D2)

Auto mode is entered either by pressing the AUTO push button or from channel sweep when a STOP is detected. Current Channel information is stored in the appropriate ER1400 address.

The FINE TUNE number stored is the current FINE TUNE number plus 20 FINE TUNE steps. This is equivalent to off-setting the frequency by −1MHz to give a symmetrical AFC capture range. Note: The above −1MHz offset is a maximum value. If by off-setting by −1MHz a channel boundary is crossed the offset is reduced to stay within the current channel.

The AFT bit is stored as a 1 to indicate Auto mode is selected. To exit from the 'Auto' mode and cancel the AFT bit, either the Fine Tune Up, Fine Tune Down, Channel Tens or Channel Units switch must be operated.

In Auto mode if UP is high the Fine Tune number is decremented by one every 12ms until UP goes low. Similarly if DOWN is high the Fine Tune number is incremented by one until it goes low. The maximum tuning range is −3.95MHz, +4MHz around the allocated channel frequency. No roll over occurs when these limits are reached, i.e. the system will only tune down from the +4MHz limit and up from the −3.95MHz limit.

Auto Fine Tune Indicator (D7)

This is a LED which is ON when the system is operating in the AUTO mode. The state of the LED is determined by the AFT bit from the ER1400.

Mute — (B5)

The Mute signal is normally high but goes active (low) for 600ms each time TUNE data is transferred to the synthesizer i.e. during a channel or program change or when the power is initially switched on. In the Channel sweep mode the MUTE is active continuously from the start of sweep until 600ms after a STOP is detected. The Mute does not go active if only Fine Tune information is transferred to the synthesizer.

The Mute output serves to mute the sound of the television when disturbances are made to the tuning.

OSC

This is an RC network which provides the basic oscillator frequency for the PIC1650-020. A 47K potentiometer is provided to allow accurate setting of the frequency to 1.0MHz.

Channel-Frequency Conversion

The channel data read from the ER1400 is converted by the PIC1650-020 into Frequency, Band and Offset information. The table below lists the Frequency Number (Q), Band (B) and Offset (R) allocated to each of the 100 channels.

For example the Tune data for channel 21 is as follows:—

Q = 514
B = 2
R = 17

This information is transferred to the synthesizer in the Tune Data format specified earlier. If the Fine Tune data is set to 128 and transferred to the synthesizer then the local oscillator will be tuned to a frequency of 510.15MHz.

TUNING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature .... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} .... −0.3V to +12V

Standard Conditions (unless otherwise noted):

Operating Temperature (Ambient) T_A = 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.5	—	7	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10	V	
Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (see Note 1)
All Inputs						
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
I/O Ports With Internal Pull-up						
Input High Voltage	V_{IH}	2.4	—	V_{DD}	V	
$\overline{\text{MCLR}}$, $\overline{\text{RTCC}}$ & OSC						
Input High Voltage	V_{IH}	$V_{DD}-1$	—	V_{DD}	V	
All Outputs Except CLK OUT						
Output Low Voltage	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA (see Note 2, 3, 4) V_{XX} = 4.5V
	—	—	—	0.90	V	I_{OL} = 5mA (see Note 2, 3, 4) V_{XX} = 4.5V
	—	—	0.50	—	V	I_{OL} = 5mA (see Note 2, 3, 4) V_{XX} = 9V
	—	—	0.9	—	V	I_{OL} = 10mA (see Note 2, 3, 4) V_{XX} = 9V
CLK OUT						
Output Low Voltage	V_{OL}	—	—	0.45	V	V_{XX} = 9.0V I_{OL} = 1.6mA (see Note 2, 3, 4)
All Outputs With Internal Pull Up						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = 100μA (see Note 2, 3, 4)
All I/O Ports With Internal Pull Up						
Input Low Current	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V (see Note 4)
Input High Current	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V (see Note 4)
$\overline{\text{MCLR}}$, $\overline{\text{RTCC}}$						
Input Leakage Current	I_{LC}	−10	—	10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$ (see Note 4)
I/O Ports With Open Drain Outputs						
Input High Voltage	V_{IH}	2.4	—	V_{XX}	V	
Input Leakage Current	I_{CL}	−10	—	10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{XX}$ (see Note 4)

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
OSC						
Oscillator Frequency	f	0.2	—	1	MHz	
Instruction Cycle Time	t_{CY}	4	—	20	μs	(see Note 6)
CLK OUT & I/O Ports with Internal Pull Up						
Rise Time	t_R	—	—	200	ns	1 TTL Load + 100pf
Fall Time	t_F	—	—	200	ns	1 TTL Load + 100pf
I/O Ports with Internal Pull Up						
Output Mode						
CLK OUT to Data Valid	t_{PD}	0	500	.800	ns	
Input Mode						
Data Set Up Time	t_S	0	—	¼ t_{CY}	ns	
Data Hold Time	t_h	0	—	25ns	ns	
$\overline{\text{RTCC}}$ Input						
Period	t_{RT}	t_{CY}	—	—	μs	
High Pulse Width	t_{RT1}	½ t_{CY}	—	—	μs	(see Note 7)
Low Pulse Width	t_{RTH}	½ t_{CY}	—	—	μs	

NOTES:
1. Maximum I_{XX} occurs when all I/O ports are high.
2. Total I_{OL} for all outputs (I/O ports + CLK OUT) must not exceed 175mA.
3. V_{XX} supply drives I/O ports. The V_{DD} supply drives CLK OUT.
4. Positive Current indicates current flow into the device. Negative Current indicates current flow out of the device.
5. Oscillator circuit as shown in Fig. 1.
6. Both the instruction Cycle Time and CLK OUT period are equal to four times the oscillator frequency i.e. t_{CY} = 4/f secs.
7. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{\text{RTCC}}$ input, CLK OUT may be directly tied to the $\overline{\text{RTCC}}$ without any loss of counts.

CHANNEL FREQUENCY ALLOCATIONS

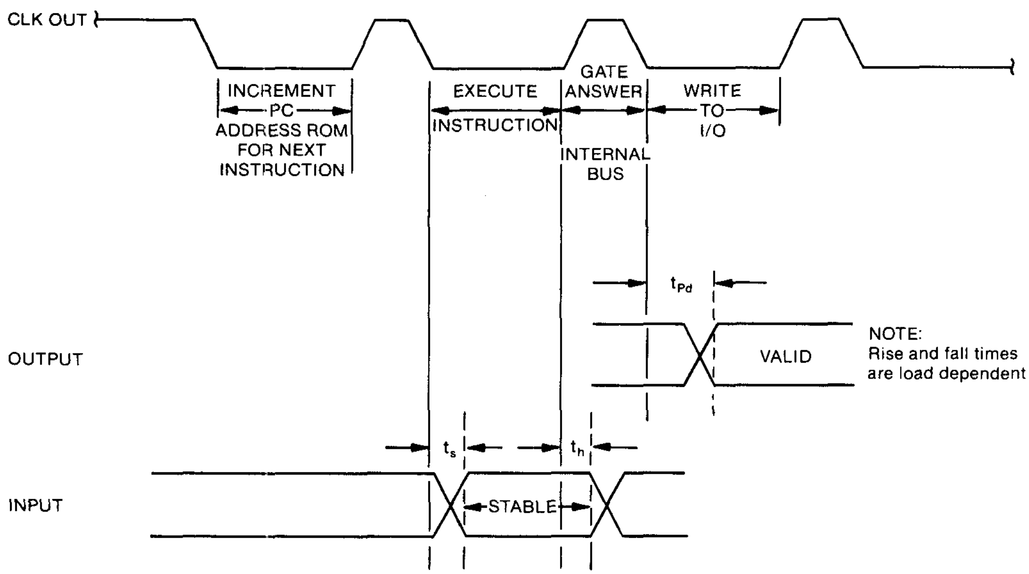
Channel Number	Channel Name	L.O. Freq MHz	Band	Q (Freq) Number	R (Offset) Number	Band		Channel Width
						AY-3-2012 Output	B	
00	1	80.15	1	84	17	BAND 1	0	7MHz
01	1	80.15	1	84				
02	2	87.15	VHFI	91				
03	3	94.15		98				
04	4	101.15	CCIR	105				
05	5	214.15		218		BAND 3	1	
06	6	221.15		225				
07	7	228.15		232				
08	8	235.15	VHF III	239				
09	9	242.15	CCIR	246				
10	10	249.15		253				
11	11	256.15		260				
12	12	263.15		267				
13	A1	108.15		112		BAND 1	0	
14	B1	115.15		119				
15	C1	122.15		126				
16	D1	129.15		133				
17	E1	136.15		140				
18	F1	85.15		89				
19	G1	98.15		102				
20	H1	132.15		136				
21	21	510.15		514		UHF	2	8MHz
22	22	518.15		522				
23	23	526.15		530				
24	24	534.15		538				
25	25	542.15		546				
26	26	550.15		554				
27	27	558.15		562				
28	28	566.15	UHF	570				
29	29	574.15	CCIR	578				
30	30	582.15		586				
31	31	590.15		594				
32	32	598.15		602				
33	33	606.15		610				
34	34	614.15		618				
35	35	622.15		626				
36	36	630.15		634				
37	37	638.15		642				
38	38	646.15		650				
39	39	654.15		658				
40	40	662.15		666				
41	41	670.15		674				
42	42	678.15		682				
43	43	686.15		690				
44	44	694.15		698				
45	45	702.15		706				
46	46	710.15		714				
47	47	718.15		722				
48	48	726.15		730				
49	49	734.15	UHF	738				
50	50	742.15	CCIR	746				
51	51	750.15		754				
52	52	758.15		762				
53	53	766.15		770				
54	54	774.15		778				
55	55	782.15		786				
56	56	790.15		794				
57	57	798.15		802				
58	58	806.15		810				
59	59	814.15		818	17	UHF	2	8MHz

CHANNEL FREQUENCY ALLOCATIONS

Channel Number	Channel Name	L.O. Freq MHz	Band	Q (Freq) Number	R (Offset) Number	Band		Channel Width
						AY-3-2012 Output	B	
60	60	822.15		826	17	UHF	2	8MHz
61	61	830.15		834				
62	62	838.15		842				
63	63	846.15		850				
64	64	854.15		858				
65	65	862.15		866				
66	66	870.15		874				
67	67	878.15		882				
68	68	886.15		890				
69	69	894.15		898				
70	70	902.15	UHF	906				
71	71	910.15	CCIR	914	17		2	
72	A	92.65		96	7	BAND 1	0	7MHz
73	B	101.15		105	17		0	
74	C	121.15		125	17		0	
75	D	214.15	ITALIAN	218	17	BAND 3	1	
76	E	222.65		226	7			
77	F	231.15		235	17			
78	G	240.15		244				
79	H	249.15		253				
80	S1	144.15		148				
81	S2	151.15		155				
82	S3	158.15		162				
83	S4	165.15		169				
84	S5	172.15		176				
85	S6	179.15		183				
86	S7	186.15		190				
87	S8	193.15		197				
88	S9	200.15		204				
89	S10	207.15	GERMAN	211				
90	S11	270.15	CABLE	274				
91	S12	277.15		281				
92	S13	284.51		288				
93	S14	291,15		295				
94	S15	298.15		302				
95	S16	305.15		309				
96	S17	312.15		316				
97	S18	319.15		323				
98	S19	326.15		330				
99	S20	333.15		337	17	BAND 3	1	7MHz

TUNING

I/O TIMING



TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE

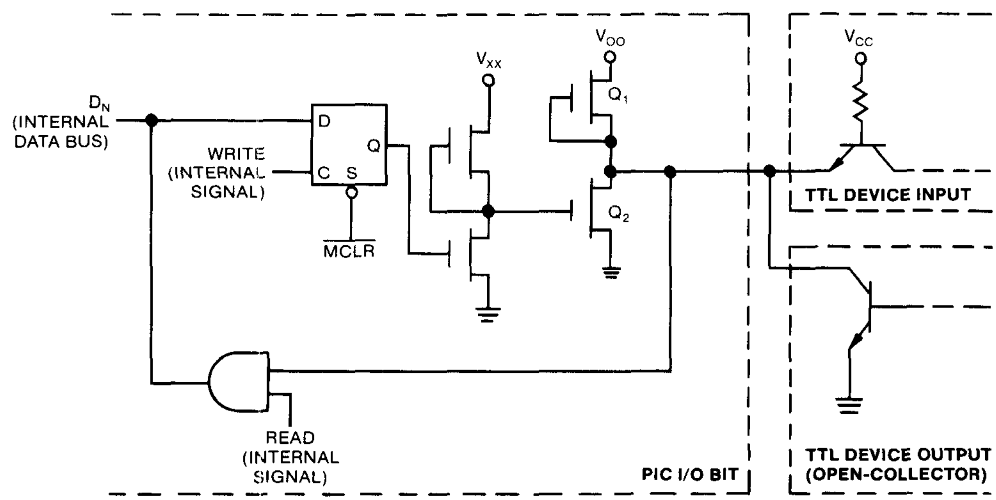
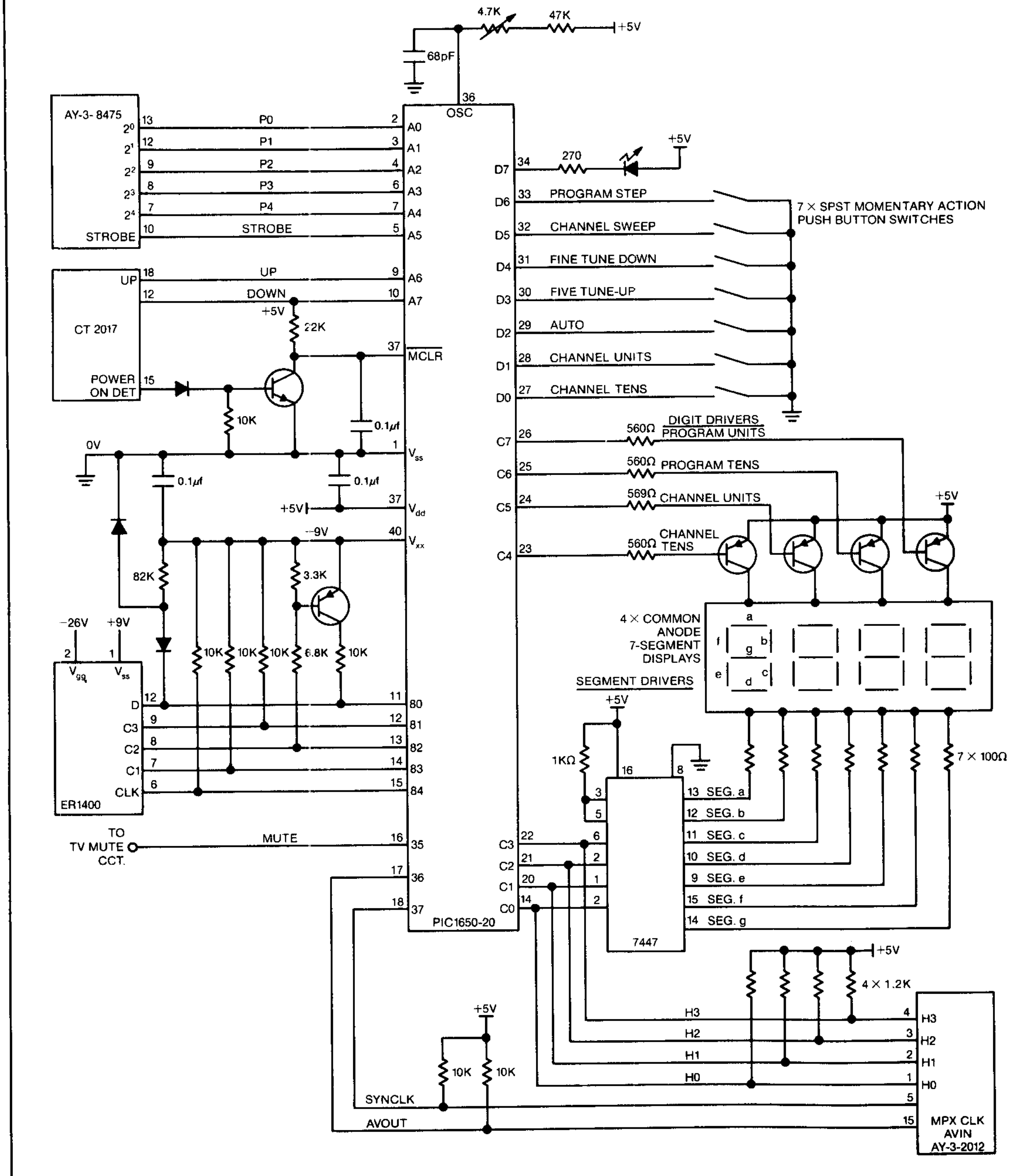


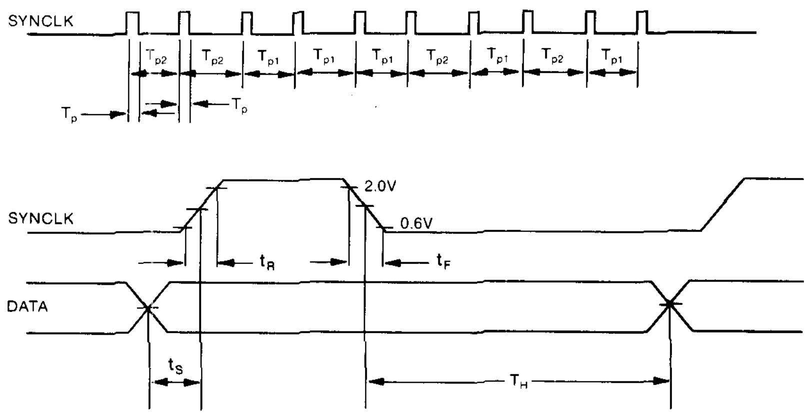
Fig. 1 I/O TIMING AND INTERFACE

TUNING



NOTES:
1. I/O's B0, B1, B2, B3, B4, B5, C0, C1, C2, C3 & D7 have open drain outputs.
2. Unless otherwise noted:
   a. Diodes are IN914
   b. NPN Transistors are 2N3904
   c. PNP Transistors are BC327

Fig. 2 CIRCUIT DIAGRAM



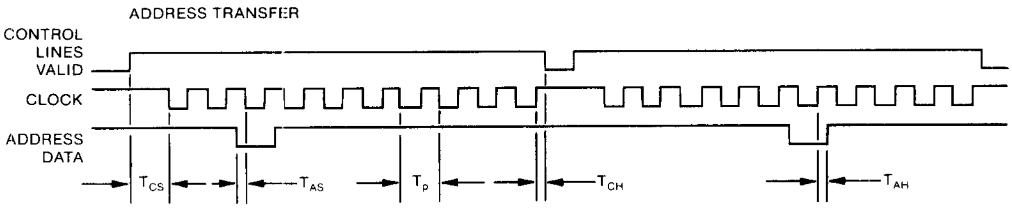
Parameter		Notes
Clock Pulse Width	T_p	4μs
Clock Period	T_{p1}	56μs
	T_{p2}	44μs
Data Set Up Time	t_s	4μs
Data Hold Time	T_m	>36μs
Clock or Data Rise Time	t_r	200ns
Clock or Data Fall Time	t_f	200ns

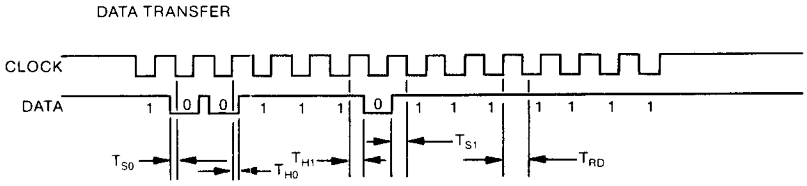
NOTES:

1. Rise and Fall times are maximum values. Other times are typical values with a tolerance of ± 250ns.
2. Times other than rise or fall times are based on a PIC1650 clock frequency of 1MHz.
3. Logic Levels: '0' <0.5V; '1' > 2.0V.

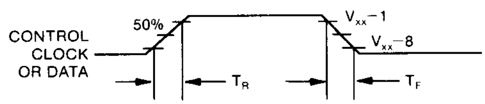
Fig. 3 PIC1650 — TIMING DIAGRAMS

TUNING





Parameter		Value
Clock Period	T_p	72µs
Clock Duty Cycle		50%
Control Set Up Time	T_{CS}	52µs
Control Hold Time	T_{CH}	4µs
Address Set Up Time	T_{AS}	8µs
Address Hold Time	T_{AH}	4µs
Write Data Set Up Time		
Logic 0	T_{S0}	16µs
Logic 1	T_{S1}	32µs
Write Data Hold Time		
Logic 0	T_{H0}	4µs
Logic 1	T_{H1}	20µs
Read Data sample Time	T_{RD}	36-40µs
Control or Clock Rise Time	t_R	1µs
Control or Clock Fall Time	t_F	1µs
Data Rise Time	T_R	8µs
Data Fall Time	T_F	4µs



NOTES:

1. Rise and fall times are maximum values. Other times are typical values with a tolerance of ±250ms. Times are measured to 50% values.
2. Times other than rise and fall times are based on a PIC1650 clock frequency of 1MHz.
3. Address transfer is shown for ER1400 address of 74.
4. ER1400 Erase/Write cycles—continuous clock pulses for 18.5ms.
5. Logic Levels: '0' <(V_{XX}−8) Volts; '1' >(V_{XX} −1) Volts.

Fig. 4 PIC1650/ER1400 TIMING DIAGRAMS