TV Time/Channel Display Circuits

FEATURES

- Channel Display 0 to 15 or 1 to 16 or 00 to 99.
- 4 Digit Clock Display option.
- Color character on black background or color character on color background.
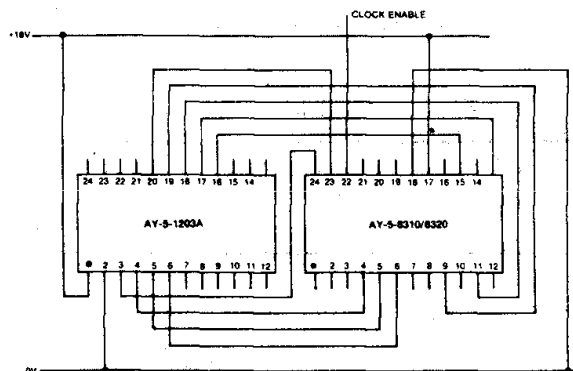- 14 or 24 DIL package.

OPTIONS

Part Number	Channel	Time
AY-5-8300	0-15	No
AY-5-8301	1-16	No
AY-5-8310/11	0-15 or 00-99	Yes
AY-5-8320/21/22/24	1-16	Yes*

*The AY-5-8320/21/22/24 are capable of either simultaneous or separate time and channel display and have automatic display enable.
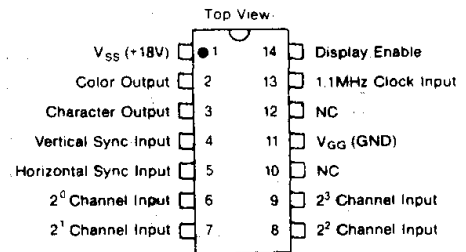
DESCRIPTION

The AY-5-8300 series is a family of MOS circuits designed to display channel and time information on the screen of a TV set. The information is displayed as color characters on a black or color background. Channel information is displayed either as a single character 0 to 15 or 1 to 16 or as a dual character 00 to 99. Time is provided as a 4 digit hours and minutes display. The display is positioned at the top right hand corner or at the bottom center of the screen; the display may be permanent or momentary. Any of the AY-5-8300 series except the AY-5-8324 may be used for either 525 or 625 line systems; the AY-5-8324 is for use with 625 line systems only.
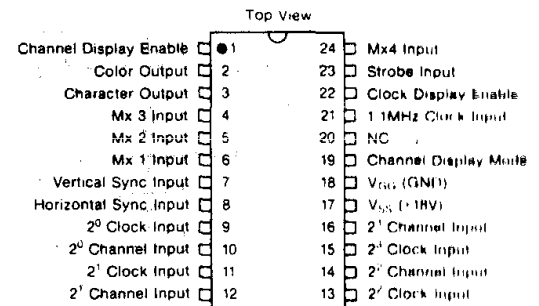
INTERCONNECT DIAGRAM FOR TV TIME DISPLAY

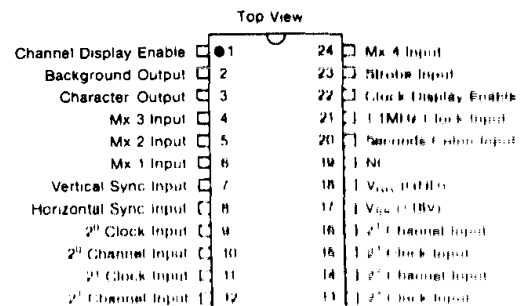## PIN CONFIGURATION

14 LEAD DUAL IN LINE

AY-5-8300/01

Top View

Pin			Pin
V_{SS} (+18V)	1	14	Display Enable
Color Output	2	13	1.1MHz Clock Input
Character Output	3	12	NC
Vertical Sync Input	4	11	V_{GG} (GND)
Horizontal Sync Input	5	10	NC
2^0 Channel Input	6	9	2^3 Channel Input
2^1 Channel Input	7	8	2^2 Channel Input

24 LEAD DUAL IN LINE

AY-5-8310/11

Top View

Pin			Pin
Channel Display Enable	1	24	Mx4 Input
Color Output	2	23	Strobe Input
Character Output	3	22	Clock Display Enable
Mx 3 Input	4	21	1.1MHz Clock Input
Mx 2 Input	5	20	NC
Mx 1 Input	6	19	Channel Display Mode
Vertical Sync Input	7	18	V_{GG} (GND)
Horizontal Sync Input	8	17	V_{SS} (+18V)
2^0 Clock Input	9	16	2^3 Channel Input
2^0 Channel Input	10	15	2^3 Clock Input
2^1 Clock Input	11	14	2^2 Channel Input
2^1 Channel Input	12	13	2^2 Clock Input

AY-5-8320/21/22/24

Top View

Pin			Pin
Channel Display Enable	1	24	Mx 4 Input
Background Output	2	23	Strobe Input
Character Output	3	22	Clock Display Enable
Mx 3 Input	4	21	1.1MHz Clock Input
Mx 2 Input	5	20	Horizontal Sync Input
Mx 1 Input	6	19	NC
Vertical Sync Input	7	18	V_{GG} (GND)
Horizontal Sync Input	8	17	V_{SS} (+18V)
2^0 Clock Input	9	16	2^3 Channel Input
2^0 Channel Input	10	15	2^3 Clock Input
2^1 Clock Input	11	14	2^2 Channel Input
2^1 Channel Input	12	13	2^2 Clock Input

PIN FUNCTIONS

Name	Function
ALL TYPES:	
Vertical Sync Input	Resets the circuit at the end of each frame. At logic '0' during vertical flyback.
Horizontal Sync Input	Activates the line counter. At logic '0' during horizontal flyback.
1.1 MHz Clock Input	Determines character position and width. Must be synchronized by horizontal sync pulse to prevent ragged edges on character.
Channel Inputs 2^0-2^3	

Code 2^3 2^2 2^1 2^0	Display AY-5-8300	Display AY-5-8301/20/21/22/24	Display AY-3-8310/11
0 0 0 0	0	1	0 0*
0 0 0 1	1	2	1 1
0 0 1 0	2	3	2 2
0 0 1 1	3	4	3 3
0 1 0 0	4	5	4 4
0 1 0 1	5	6	5 5
0 1 1 0	6	7	6 6
0 1 1 1	7	8	7 7
1 0 0 0	8	9	8 8
1 0 0 1	9	10	9 9
1 0 1 0	10	11	10 —
1 0 1 1	11	12	11 —
1 1 0 0	12	13	12 —
1 1 0 1	13	14	13 —
1 1 1 0	14	15	14 —
1 1 1 1	15	16	15 —

*00-99 MODE.

Name	Function
AY-5-8300/01	
Display Enable	When taken to logic '0', the display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
AY-5-8300/01/10/11	
Character Output	Defines the background border and the character.
Color Output	Determines the character color. Goes to logic '1' during a character block.
AY-5-8310/11	
Channel Display Enable	When taken to logic '0', the channel display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
Clock Display Enable	When taken to logic '0', the clock display is enabled.
Channel Display Mode	When at logic "0", the 0-15 channel mode is selected; logic "1" for 00-99 channel mode.
AY-5-8310/11/20/21/22/24	
Clock Inputs 2^0-2^3	Multiplexed 4 digit BCD clock data inputs such as available from the AY-5-1203A clock circuit.
Mx1-Mx4	Multiplex Inputs, at logic '1' during multiplex time slot. For the AY-5-8310/11, when operating in the 00-99 channel mode, Mx1 and Mx2 time slots are used.
Strobe Input	This input must go to a logic '1' during the middle of each Mx time slot to load the clock data into the chip.
AY-5-8320/21/22/24	
Character Output	Defines the character outlines. At logic '1' when displaying a character.
Background Output	Defines the background block. At logic '1' when outputting background.
Channel Display Enable	When taken to logic '1', the channel display is enabled. The display is automatically enabled when the channel is changed.
Clock Display Enable	When taken to logic '1', the clock display is enabled.
Seconds Colon Input	This input controls the colon between the hours and minutes display. When at logic '0', the colon is blanked. If connected to the DP output of the AY-5-1203A clock circuit, the colon will flash once per second.

OPERATION

The display is positioned digitally in both the vertical and horizontal directions. The vertical position is determined by counting horizontal sync pulses (the counting is initiated by the vertical sync pulse). The timing relationships are shown in Figs. 8a and 8b. Additionally, for the AY-5-8320/21/22/24, the time display is positioned 35 lines further down so that it appears immediately below the channel display.

In the horizontal direction the display is positioned by counting pulses from an external 1.1 MHz oscillator which is synchronized with the horizontal sync pulse to prevent ragged edges on each character.

Each character is made up of 15 dots in a 3×5 matrix. With a one dot border around each character a total matrix of 35 dots in a 5×7 format is utilized. Each dot lasts 0.9µ'sec in the horizontal direction and is 5 lines high. This gives a rectangular dot and characters as shown in Figs. 1a and 1b.

The various channel/time display formats are illustrated in Figs. 4, 6 and 7. The display positioning on the TV screen is shown in Figs. 6a and 6b.

In the AY-5-8300/01/10/11, the character display is controlled by two outputs. Character and Color. The video channels are controlled in the following manner:

(a) Black/white display

Character	Color	
0	0	Normal picture
1	0	Black (luminance channel full off)
1	1	Black
0	1	White

(b) Black/Yellow display

Character	Color	Normal picture
1	0	Black (luminance full off)
1	1	Black (luminance full off and blue suppressed)
0	1	Yellow (luminance full on and blue suppressed)

Other color displays are generated by suppressing one or two chrominance channels.

In the AY-5-8320/21/22/24, one video output defines the characters and the other a background block. Using these outputs, a display of any color character on a background of any color may be obtained.

The channel data is input on four lines; in the 0—15 or 1—16 channel mode, this information is applied in binary from a diode encoder attached to the varactor tuning drivers. Binary numbers greater than 9 are detected and displayed as a two digit character.

In the clock mode, data is entered on a 4 line BCD bus multiplexed into 4 time slots. A strobe signal occurring in the middle of each time slot is used to read the data into the chip. When the AY-5-1203A clock is used it can be directly connected to the AY-5-8310/11/20/21/22/24 with no external components The AY-5-8310/11 displays the time with hours and minutes (Fig. 4); the AY-5-8320/21/22/24 displays the time with hours, minutes and a flashing colon for seconds (Fig. 5).
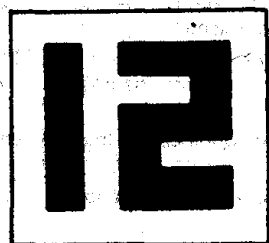
In the 00-99 channel mode the data is entered as a two digit BCD number in Multiplex time slots 1 and 2 in the same manner as the clock formation.
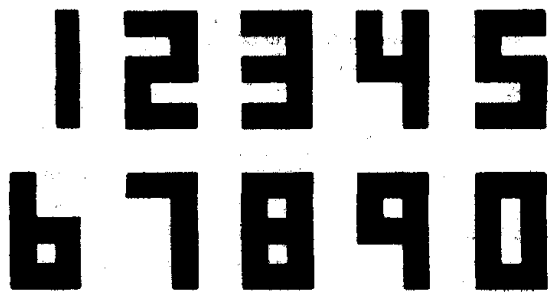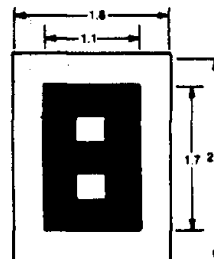

Fig. 1a CHARACTER SET
(AY-5-8300/10)
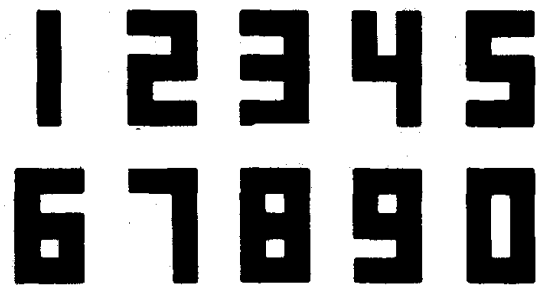
Fig. 1b CHARACTER SET
(AY-5-8301/11/20/21/22/24)

Fig. 2 CHANNEL DISPLAY

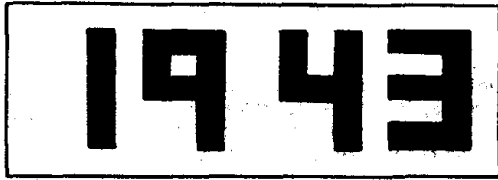**Fig. 3 CHARACTER SIZE**
(25/26 INCH SCREEN)
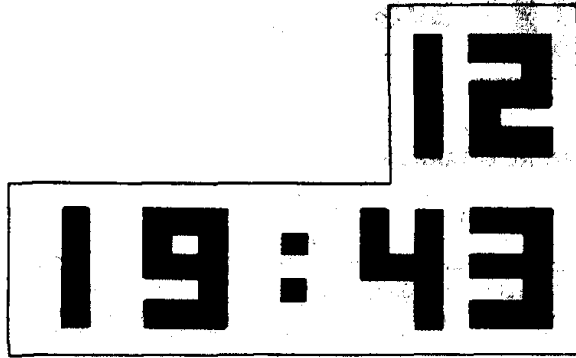
Fig.4 TIME DISPLAY (AY-5-8310/11)

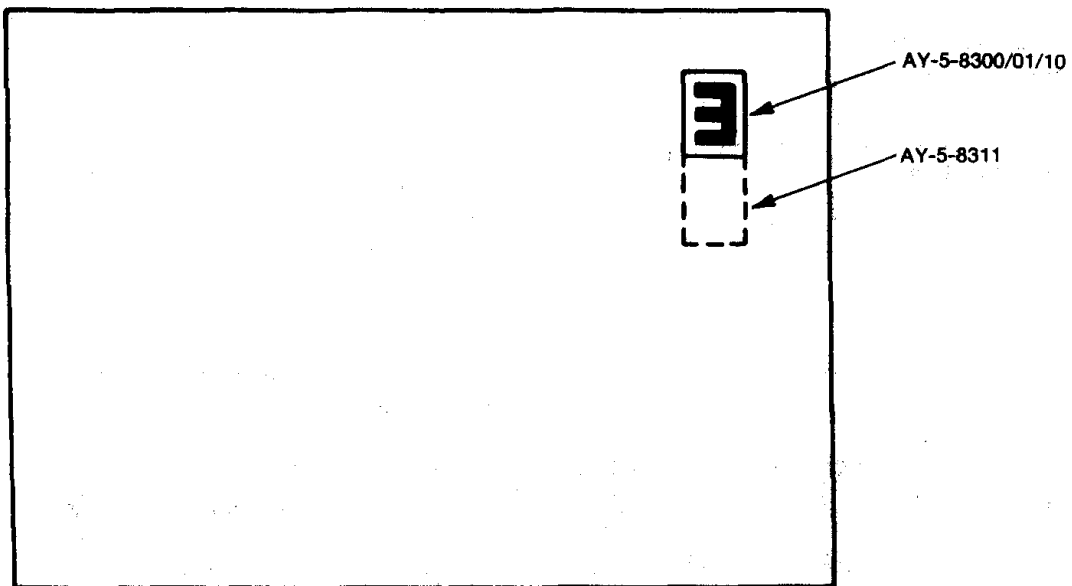**Fig.5 TIME AND CHANNEL DISPLAY (AY-5-8320/21/22/24)**

AY-5-8300/01/10

AY-5-8311

Fig.6a DISPLAY POSITION-CHANNEL (AY-5-8300/01/10/11) OR TIME (AY-5-8310/11)
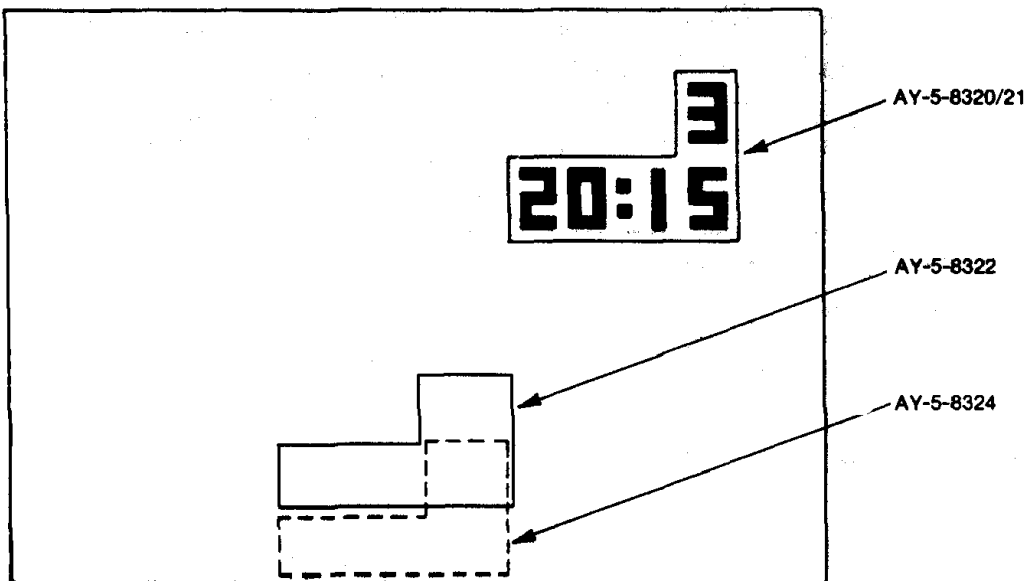
AY-5-8320/21

AY-5-8322

AY-5-8324

Fig.6b DISPLAY POSITION-CHANNEL (AY-5-8300/01/10/11)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{ss} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . . 0°C to +85°C
Storage temperature range. . . . . : . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

### Standard Conditions (unless otherwise noted)

$V_{GG} = 0V$
$V_{ss} = +17V$ to $+19V$
Operating Temperature (T_A) = 0°C to +85°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	$V_{ss}-5$	—	$V_{ss}+0.5$	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	7	Volts	
Logic '1'	$V_{ss}-1.5$	—	$V_{ss}+0.3$	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	7	Volts	
Logic '1'	$V_{ss}-5$	—	$V_{ss}+0.3$	Volts	
Rise & Fall Time	—	—	300	ns	10% to 90%
Pulse width	250	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	$V_{ss}-5$	—	$V_{ss}+0.5$	Volts	
Leakage	—	—	10	μA	$V_{IN} = (V_{ss}-19)$ Volts
Display Enable Inputs					
Switch point positive edge	$V_{ss}-8$	—	$V_{ss}-5$	Volts	
Outputs					
On resistance	—	—	1.5	kΩ	$V_{OUT} = V_{ss}-2V$
Off leakage	—	—	1	μA	$V_{OUT} = 0V$
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power: AY-5-8300/01/10	—	—	400	mW	$V_{ss} = +19V$
AY-5-8320	—	—	750	mW	$V_{ss} = +19V$

**Typical values are at +25°C and nominal voltages.
NOTE:
1. These inputs are diode clamped to V_{ss}. Maximum clamp current 50μA.
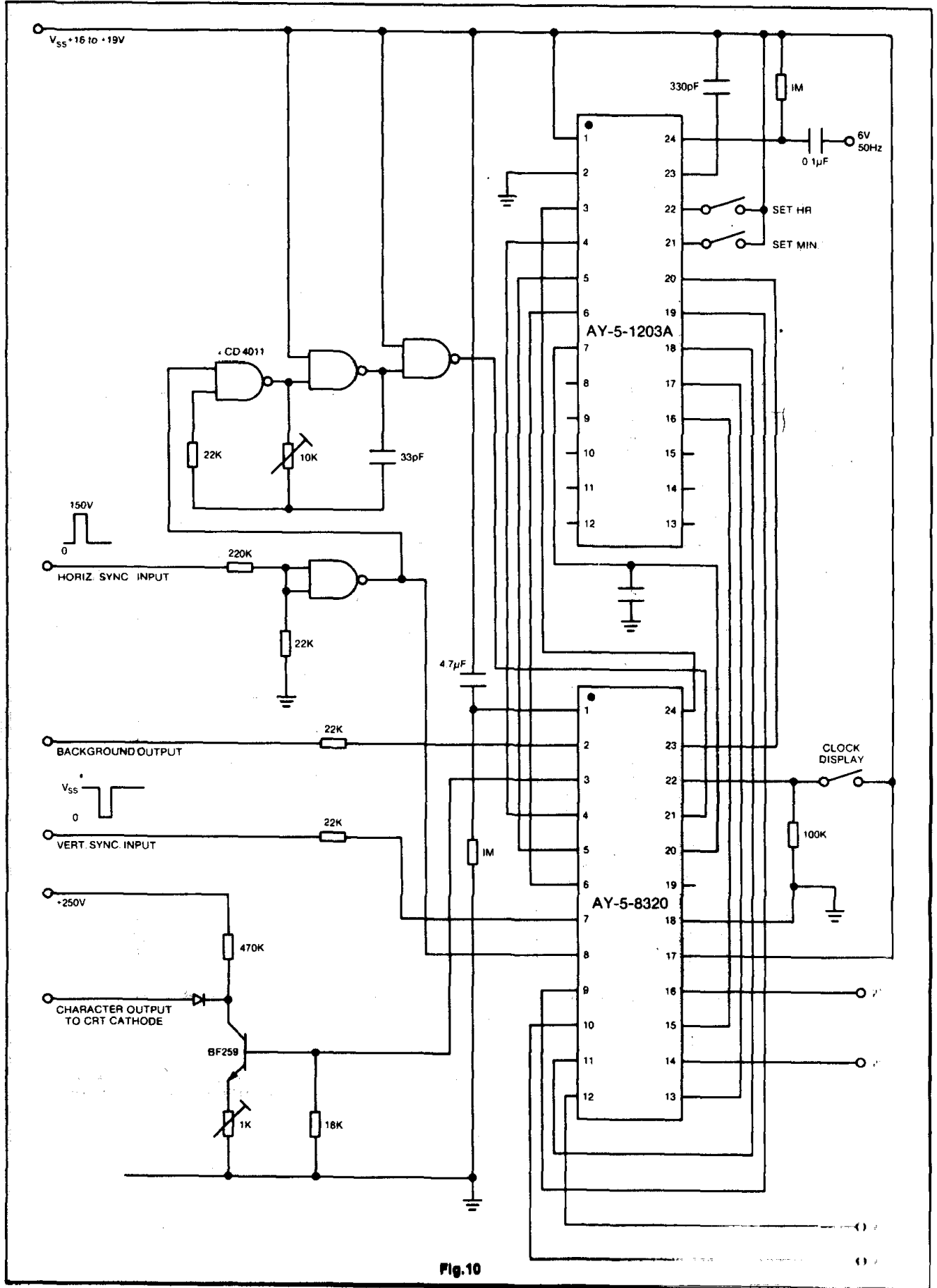

Fig. 7 INPUT WAVEFORMS
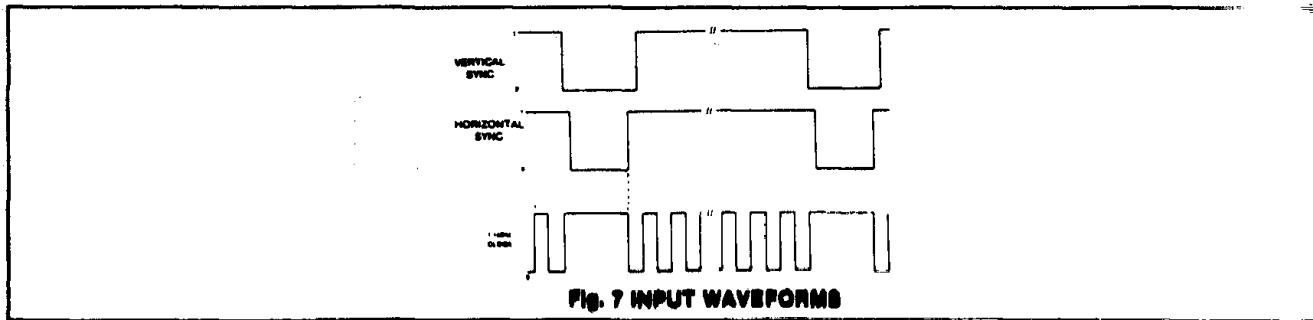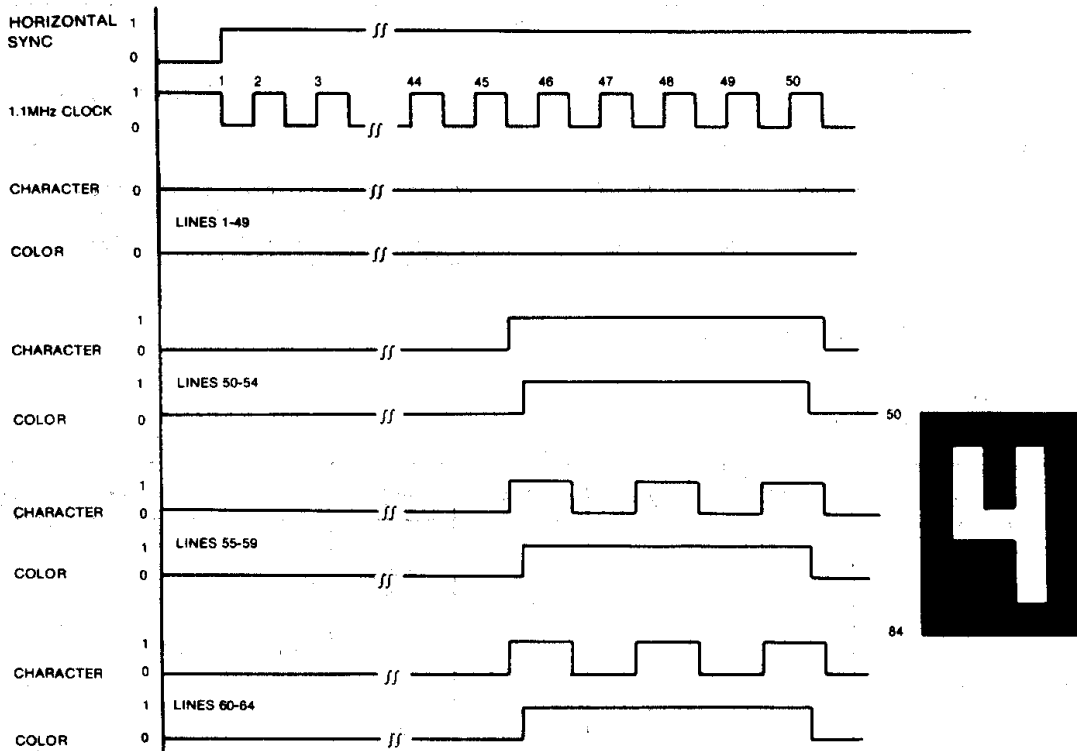
Fig. 8a OUTPUT WAVEFORMS (AY-5-8300/01/10)
(AY-5-8311 AS ABOVE BUT DISPLAY STARTS AT LINE 85.)
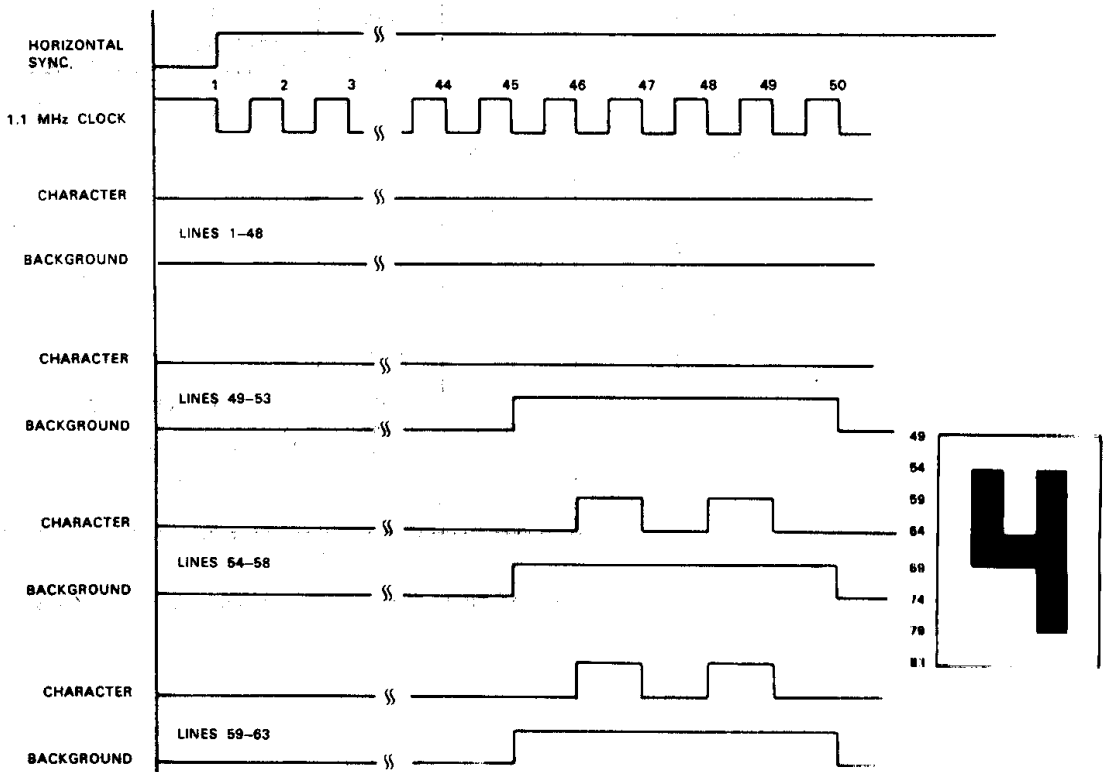
Fig. 8b OUTPUT WAVEFORMS (AY-5-8320/21)
(AY-5-8322 AS ABOVE BUT DISPLAY STARTS AT LINE 165.
AY-5-8324 AS ABOVE BUT DISPLAY STARTS AT LINE 330.)

Fig.10